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AMENDMENTS TO THE CLAIMS

This listing and version of the claims replace all prior listing and versions of the claims.

Listing of Claims:

1. (Currently Amended) A single transistor random access memory cell, comprising:

a transfer gate over a substrate having a recess;

a storage capacitor ~~with a storage node having an MOS native device with a near zero threshold voltage to form an inversion layer~~ having a capacitor plate horizontally adjacent to the transfer gate; and

a shallow trench isolation, STI, insulator within the recess of the substrate, the STI insulator having a ~~reduced step~~ height smaller than a depth of the recess of the substrate~~below that of an overdoped OD sidewall of a substrate insulator; and~~, wherein the

a capacitor plate ~~covering~~covers the STI insulator and conformally covers a sidewall of the recess of the substrate~~the overdoped OD sidewall~~.

2. (Original) The cell as in claim 1, further comprising:

an inversion region beneath the transfer gate, which is formed by diffusion of the inversion layer.

3. (Cancelled).

4. (Original) The cell as in claim 1, wherein

the transfer gate and a capacitor plate being closer together than a minimum line width of a single photomask.

5. (Original) The cell as in claim 4, further comprising:

a dielectric spacer between the transfer gate and the capacitor plate.

6. (Cancelled)

7. (Currently amended) The cell as in claim ~~6~~1, further comprising:

an inversion region beneath the transfer gate, which is formed by diffusion of the inversion layer.

8. (Withdrawn – Currently amended) The cell as in claim ~~6~~30, wherein

the transfer gate has another MOS native device forming an inversion region at a near zero threshold voltage.

9. (Currently amended) The cell as in claim ~~6~~1, wherein

the transfer gate and a~~t~~the capacitor plate ~~being~~are closer together than a minimum line width of a single photomask.

10. (Currently amended) The cell as in claim ~~6~~1, further comprising:

a dielectric spacer between the transfer gate and the capacitor plate.

11. (Currently amended) The cell as in claim 1, further comprising:

~~a shallow trench isolation, STI, insulator having a reduced step height below that of an OD sidewall of a substrate insulator;~~

~~the transfer gate and the capacitor being in an active area of the substrate;~~

an external MOS native device external to ~~the~~an active area of the substrate, the external MOS native device forming an inversion layer at near zero threshold voltage, wherein the transfer gate and the capacitor are in an active area of the substrate,[[;]] and

a~~t~~the capacitor plate ~~covering~~covers the STI insulator and the external MOS native device.

12. (Original) The cell as in claim 11, further comprising:

an inversion region beneath the transfer gate, which is formed by diffusion of the inversion layer.

13. (Withdrawn) The cell as in claim 11, further comprising:

the transfer gate having an MOS native device forming an inversion region at a near zero threshold voltage.

14. (Currently amended) The cell as in claim 11, ~~further comprising~~: wherein the transfer gate and athe capacitor plate ~~being~~are closer together than a minimum line width of a single photomask.

15. (Original) The cell as in claim 14, further comprising:
a dielectric spacer between the transfer gate and the capacitor plate.

16-29 (Cancelled)

30. (New) The cell as in claim 1, wherein the capacitor has a storage node having an MOS native device with a near zero threshold voltage to form an inversion layer.